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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,069	12/09/2003	Pravinkumar Premakanthan	1280-SC12966ZC	3764

34814 7590 05/17/2006

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EXAMINER	
CHU, MICHAEL	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,069	PREMAKANTHAN ET AL.	
	Examiner	Art Unit	
	Michael Chu	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 25* is/are allowed.

6)☒ Claim(s) *1-10,12-24 and 26-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed February 24, 2006 have been fully considered but they are not persuasive.

In response to applicant's argument in claim 1 that reference fails to teach, mention, disclose or suggest a power detector coupled to an output of the gain control stage, the power detector to detect a ramp of the amplified signal and to provide an indication of the ramp.

Examiner respectfully disagrees, and further cited in Epperson et al. (US Publication# 2003/0040343) teaches/mentions an adjustable power control signal 74 (Vramp) and a voltage regulator 70 within the power control circuitry 46 (0034, lines 1-9, 0035, lines 1-14, See Parts 74, 70, 78, 46 of Figure 2), where the voltage regulator controls the regulated output 78. The same regulated output 78 is regulates voltage supplied to the second and third amplifier stages 62, 64, respectively of the power amplifier circuitry 44 (0035, lines 1-14, particularly lines 7-11, See Parts 78, 62, 64, 44 of Figure 2). Epperson et al. shows an amplified RF signal (0031, lines 1-11, 0034, lines 1-9, See Parts 60, 62, 64, 46, 44, 74 of Figure 2, See Part 32 of Figure 1), where the power amplifier circuitry 44 provides gain for the signal to be transmitted under control of the power control circuitry 46, which is preferably controlled by the control system 32 using the Vramp signal 74. The ramp up time and ramp down time of the adjustable power control signal (Vramp) must conform to the shape of the burst mask,

where the amplitude of Vramp dictates the output power (0012, lines 1-11, 0014, See Parts 46, 74 of Figure 2, 0035).

Therefore, examiner interpreted "a power detector coupled to an output of the gain control stage, the power detector to detect a ramp of the amplified signal and to provide an indication of the ramp" as broadest reasonable interpretation, and it is proper.

In response to applicant's argument in claim 17 that reference fails to teach, mention, disclose or suggest amplifying the RF signal with a gain control stage to produce an amplified signal, and detecting a ramp of the amplified signal.

Examiner respectfully disagrees, and further cited in Epperson et al. (US Publication# 2003/0040343) discloses *"an adjustable power control signal 74 (Vramp) may be received by a negative input 76 of an operational amplifier forming error amplifier 68. The output 78 of the voltage regulator 70 is fed back through the feedback network 72 and received by positive input 80 of error amplifier 68. An output signal 82 from error amplifier 68 is provided to a control input 84 of the voltage regulator that controls the regulated output 78 of voltage regulator 70. The voltage regulator 70 regulates the voltage supplied to the rails 86, 88 of the second and third amplifier stages 62, 64, respectively. These rails 86, 88 will typically be the collectors or drains of bipolar or field effect transistors forming the respective amplifier stages" (0035, See Parts 74, 76, 68, 78, 70, 72, 80, 82, 84, 86, 88, 62, 64 of Figure 2).*

Epperson et al. teaches/mentions an amplified RF signal (0031, lines 1-11, 0034, lines 1-9, See Parts 60, 62, 64, 46, 44, 74 of Figure 2, See Part 32 of Figure 1), where

the power amplifier circuitry 44 provides gain for the signal to be transmitted under control of the power control circuitry 46, which is preferably controlled by the control system 32 using the Vramp signal 74. The ramp up time and ramp down time of the adjustable power control signal (Vramp) must conform to the shape of the burst mask, where the amplitude of Vramp dictates the output power (0012, lines 1-11, 0014, See Parts 46, 74 of Figure 2, 0034-0035).

Therefore, examiner interpreted "amplifying the RF signal with a gain control stage to produce an amplified signal", and "detecting a ramp of the amplified signal" as broadest reasonable interpretation, and it is proper.

Claims 2-10 and 12-16 depend on independent claim 1 and are anticipated by Epperson et al. for the reasons stated above under base claim 1. Claims 18-24 and 26-30 depend on independent claim 17 above and are anticipated by Epperson et al. for the reasons stated above under base claim 17. Thus, the present application is not in condition for allowance.

Information Disclosure Statement

1. The Information Disclosure Statement received on 12/09/03 has been considered by Examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

2. Claims 1-10, 12-24 and 26-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Epperson et al. (US Publication# 203/0040343).

Consider Claim 1. Epperson et al. teaches a power control system comprising:

-a gain control stage configured to amplify an input signal to produce an amplified signal (0034, lines 1-9, 0031, lines 1-11, See Parts 60, 62, 64 of Figure 2);

-a power detector coupled to an output of the gain control stage, the power detector to detect a ramp of the amplified signal and to provide an indication of the ramp (0034, lines 1-9, 0035, lines 1-14, See Parts 60, 62, 64, 44, 74, 70, 78, 46 of Figure 2, 0012, lines 1-11, 0014); and

-a controller coupled to the power detector and the gain control stage (See Part 32 of Figure 1), the controller configured to adjust a supply or control voltage to the gain control stage responsive to the indication of the ramp to cause the supply or control voltage to change as the ramp varies from a predetermined ramp (0026, 0031), wherein the predetermined ramp comprises a desired waveform curve modified by a required power level (0026, 0031, 0012, 0055).

Consider Claim 17. As mentioned in rejecting claims 1, 7 and 14 above, Epperson et al. teaches a method of amplifying a radio frequency (RF) signal, the method comprising:

-amplifying the RF signal with a gain control stage to produce an amplified signal (0034, lines 1-9, 0035, lines 1-14, See Parts 74, 76, 68, 78, 70, 72, 80, 82, 84, 86, 88, 62, 64 of Figure 2;

-detecting a ramp of the amplified signal (0035, lines 1-14, 0012, lines 1-11, 0014, See Parts 74, 76, 68, 78, 70, 72, 80, 82, 84, 86, 88, 62, 64 of Figure 2);

-comparing the ramp of the amplified signal to a predetermined ramp producing an error difference, wherein the predetermined ramp comprises a desired waveform curve modified by a required power level (0026, 0031, 0012, 0055, 0012, lines 1-11, 0014);

-dynamically adjusting multiple taps of an adaptive filter based on the error difference signal producing a control signal (0017, 0029, 0034-0035, 0037, 0062);

-filtering the control signal with a loop filter that has a fixed loop bandwidth producing a filtered control signal (0009, 0011, 0017, 0040, 0055-0056, 0062); and

-controlling a control voltage of the gain control stage based on the filtered control signal (0026, 0031).

Consider Claims 2 and 18, in regards to claims 1 and 17, respectively, above. Epperson et al. teaches the power control system wherein the required power level comprises a power versus time mask and the desired waveform curve is a raised cosine wave (0012, 0055, See Figure 4).

Consider Claims 3 and 19, in regards to claims 1 and 17, respectively, above. Epperson et al. teaches the power control system wherein the required power level comprises a mask according to a predefined power versus time specification and a transient power specification (0012, 0055, See Figure 4, 0055, lines 1-4, 0050, 0059).

Consider Claim 4, in regards to claim 1 above. Epperson et al. teaches the power control system wherein the voltage is one of a supply voltage and a control voltage (0013, lines 3-5, 0026, lines 6-7, 0057, lines 1-3, 0067, lines 5-7).

Consider Claims 5 and 20, in regards to claims 1 and 17, respectively, above. Epperson et al. teaches the power control system wherein the predetermined ramp is independent of operating conditions of the power control system (0026, lines 4-8).

Consider Claim 7, in regards to claim 1 above. Epperson et al. teaches the power control system, the controller comprising:

-an error squaring unit (0060, 0008); and

-an adaptive filter coefficients calculation unit (0028, lines 11-18, 0044); and

-an adaptive filter having multiple taps coupled to the adaptive filter coefficients calculation unit (See Part 38 of Figure 1);

-wherein the ramp of the amplified signal is compared to the predetermined ramp producing an error term (0017, 0029, 0034, See Part 68 of Figure 2);

-wherein the adaptive filter coefficients calculation unit uses the error term to calculate and adjust one or more of the multiple taps of the adaptive filter (0017, 0029, 0034-0035, 0037, 0062);

-wherein an output of the adaptive filter is fed into a loop filter that accumulates the output signal (See Part 38 of Figure 1, 0028, lines 11-15, See Rf(out) of Figure 2).

Consider Claims 8 and 22, in regards to claims 7 and 17, respectively, above. Although Epperson et al. teaches the power control system, Epperson et al. does not specifically teach the system wherein the adaptive filter coefficients calculation unit utilizes a least mean square (LMS) adaptive algorithm. It is inherent in the art for a power control system to utilize a least mean square adaptive algorithm.

Consider Claims 9 and 23, in regards to claims 7 and 17, respectively, above. Although Epperson et al. teaches the power control system, Epperson et al. does not specifically teach the system wherein the adaptive filter coefficients calculation unit

utilizes a recursive least squares algorithm. It is inherent in the art for a power control system to utilize a recursive least squares algorithm.

Consider Claims 10 and 24, in regards to claims 7 and 17, respectively, above. Epperson et al. teaches the power control system wherein the output of the adaptive filter converges to zero (0043).

Consider Claims 12 and 26, in regards to claims 7 and 17, respectively, above. Epperson et al. teaches the power control system further comprising: an activity detection circuit for producing an activity output indicating a detection of activity; wherein the activity output selects between a null signal when activity is not detected and the predetermined ramp when activity is detected to compare with the ramp of the amplified signal (0062), where the closed loop control includes an error amplifier 68 and a voltage feedback network for comparing voltage(RAMP) with a sample of the regulator output voltage.

Consider Claim 13, in regards to claim 7 above. Epperson et al. teaches the power control system further comprising a voltage control circuit coupled between the controller and the gain control stage (0031, See Part 46 of Figure 1, 0034, lines 7-9), wherein the controller produces a control signal responsive to the error term; the voltage control circuit processing the control signal to produce the supply voltage (0026, 0013, 0057).

Consider Claims 14 and 27, in regards to claims 1 and 17, respectively, above. Epperson et al. teaches the power control system further comprising:

-a loop filter (See Part 38 of Figure 1) coupled to the output of the controller for filtering an output of the controller using a fixed loop bandwidth (0009, 0011, 0017, 0040, 0055-0056, 0062), wherein the fixed loop bandwidth is independent of operating conditions, the operating conditions including variations of analog circuit elements over temperature, supply voltage, frequency band of operation (0026, lines 4-8, 0002, 0036, 0046, 0049-0050).

Consider Claims 15 and 29, in regards to claims 1 and 17, respectively, above. Epperson et al. teaches the power control system wherein the controller controls a ramp up of the amplified signal (0012, 0014).

Consider Claims 16 and 30, in regards to claims 1 and 17, respectively, above. Epperson et al. teaches the power control system wherein the controller controls a ramp down of the amplified signal (0012, 0014).

Consider Claims 6, 21 and 28, in regards to claims 5, 20 and 27, respectively, above. Epperson et al. teaches the power control system wherein the operating conditions comprise a power input level to an amplifier stage, temperature, frequency band of operation, and a battery voltage level (0026, lines 4-8, 0002, 0036, 0046, 0049-0050).

Allowable Subject Matter

Claims 11 and 25 are allowed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Chu whose telephone number is 571-272-7875. The examiner can normally be reached on Monday-Friday (8:30am-5pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 571-272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Chu
Examiner
Art Unit 2618

MC 05/01/2006

NAY MAUNG
SUPERVISORY PATENT EXAMINER